Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1 to 22 (cancelled)

Claim 23 (original): A method comprising:

receiving onto an integrated circuit from a fiber optic cable a first number of packets, at most one of the packets being received at any one time on one of a second number of input ports of the integrated circuit, the first number being greater than the second number;

segmenting the packets on a per port basis such that at any one time at most one packet is being segmented for each of the second number of input ports, the segmenting of a packet resulting in a plurality of segments;

maintaining a number of segmentation contexts such that one segmentation context is maintained per packet being segmented, and using the segmentation context to generate a trailer that is appended to one of the segments of the packet being segmented;

storing each of the segments of each of the first plurality of packets into a corresponding one of a plurality of buffers, the trailer appended to a segment being stored along with the segment into the plurality of buffers; and

retrieving from the plurality of buffers the segments of the first number of packets and outputting each segment of the first number of packets from the integrated circuit to a switch fabric in the form of a switch cell, wherein the number of segmentation contexts maintained is less than the first number.

Claim 24 (original): The method of Claim 23, wherein the input ports are logical input ports associated with a single physical input port.

Claims 25-44 (cancelled)

Claim 45 (currently amended): A multi-service segmentation and reassembly (MS-SAR) integrated circuit employing a plurality of logical input ports, the MS-SAR integrated circuit comprising:

bus interface circuitry;

a segmentation engine that receives a plurality of flows via the bus interface circuitry, each of the plurality of flows comprising a plurality of packets, the segmentation engine segmenting the packets of the flows on a per logical input port basis such that at any one time at most substantially one packet is being segmented for each of the plurality of logical input ports, the segmenting of a packet resulting in a plurality of segments; and

a memory manager,

wherein the segmentation engine passes a plurality of chunks to the memory manager, each of the chunks comprising one of the segments, the memory manager storing ~~each of the~~ each of the chunks into a corresponding memory buffer,

wherein the segmentation engine maintains at most one segmentation context per packet being segmented, and

wherein each segmentation context comprises a byte count value and a cyclic redundancy check value.

Claim 46 (previously presented): The MS-SAR integrated circuit of Claim 45, wherein the segmentation engine receives a packet as a plurality of bursts, and wherein the segmentation engine accumulates several bursts to form a segment.

Claim 47 (cancelled)

Claim 48 (previously presented): The MS-SAR integrated circuit of Claim 45, wherein the segmentation engine segments one and only one packet for each of the plurality of logical input ports.

Claim 49(previously presented): The MS-SAR integrated circuit of Claim 45, wherein the logical input ports are active logical input ports, and wherein in addition to the active logical input ports there are inactive logical input ports.

Claims 50 to 51 (cancelled)

Claim 52 (previously presented): The MS-SAR integrated circuit of Claim 45, wherein the plurality of flows pass from the bus interface circuitry, through a lookup engine, and to the segmentation engine.

Claim 53 (previously presented): The MS-SAR integrated circuit of Claim 45, wherein the segmentation engine also receives a flow of cells via the bus interface circuitry, the segmentation engine segmenting the cells into segments.

Claims 54 to 59 (cancelled)